United Monolithic Semiconductors

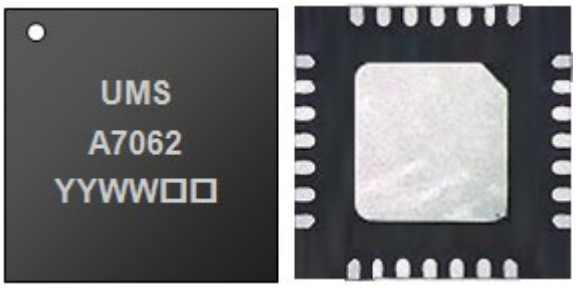
CHA7062-QCB

13-20GHz High Power Amplifier

GaN Monolithic Microwave IC in SMD leadless package

Description

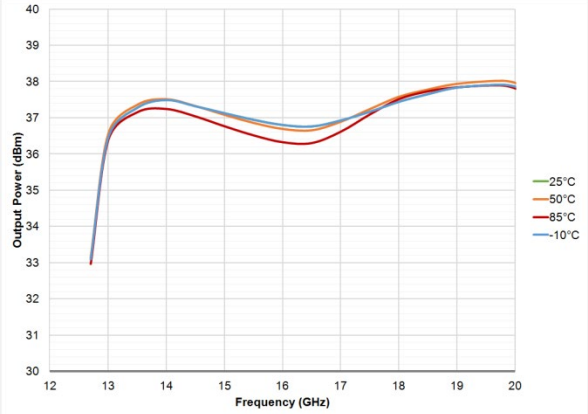
The CHA7062-QCB is a two stages monolithic GaN Power Amplifier exhibiting 5W saturated output power over 13-20GHz frequency range.
It features 17% power added efficiency and a linear gain of more than 18dB.
The circuit is realized on 150nm Gallium Nitride on Silicon Carbide (AlGaN/GaN on SiC) technology.
It is designed for Point To Point Radio and VSAT applications and is provided on low cost SMD RoHS compliant plastic package.



Main Features

- RF bandwidth: 13-20GHz
- Gain: 18dB
- Psat: 37dBm
- PAE: 17% @37dBm average Pout
- DC bias: Vd = 20Volt @ Idq = 216mA
- 28 leads QFN 5x5mm²
- MSL3

Saturated output power vs frequency



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	13		20	GHz
Gain	Linear Gain		18		dB
P_{sat}	Saturated output power		37		dBm
Idq	Total drain current		216		mA

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Specifications

Tamb.= +25°C, Vd = +20V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	13		20	GHz
Gain	Linear Gain		18		dB
ΔG	Gain variation in temperature		± 0.03		dB/°C
RL_{in}	Input return loss		-13		dB
ΔVg /ΔG	Gain Control		10		V/dB
RL_{out}	Output return loss		-9		dB
NF	Noise Figure		8		dB
PAE	Pout ≈37dBm		17		%
P_{sat}	Saturated output power		37		dBm
C/I3 @ 6dB OBO	Fundamental over Carrier @ 6 dB Output Back-off		26.5		dBc
Pdc @ 29 dBm	DC power consumption @ 29 dBm Output power		8		W
Dr	Detection dynamic range (for output power detection up to Psat)		30		dB
Vdetect	Voltage detection V_{REF}- V_{DET} up to Psat		10 to 2200		mV
Vg	DC gate Voltage		-2.85		V
Idq	Total drain current		216		mA

These values are representative of measurements performed on evaluation board as defined on the drawing in paragraph "Evaluation board".

Electrostatic discharge sensitive device observe handling precautions

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Value	Unit
Vd	Drain bias voltage	27	V
Vg	Gate bias voltage range	[-10 ; -2]	V
Id	Drain current at max. input power	2000	mA
Pin	Maximum input power	+26	dBm
Ta	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device beyond any of these limits may cause permanent damage.

Recommended Operating Parameters (2)

Tamb.= +25°C

Symbol	Parameter	Value	Unit
Vd	Drain bias voltage	20	V
Vg	Gate bias voltage	-2.85	V
Idq_stg1	1st stage drain current (North and South) without RF signal	72	mA
Idq_stg2	2nd stage drain current (North and South) without RF signal	144	mA
Pin	Maximum Input power	+20	dBm

(2) Electrical performances are defined for specified test conditions and are not guaranteed over all recommended operating conditions.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Value	Unit
Vd	9, 13, 23, 27	Drain voltage	20	V
Vg	8, 11, 25, 28	Gate voltage	-3	V
Id		DC Drain current Max. HPA drain current vs. Pin max.	216 2000	mA
Ig		DC HPA gate current Max. HPA gate current vs. Pin max.	0.03 1	mA
Vc	21	Detector voltage supply	6	Vs

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“Power ON” sequence

1. Ground the device: I_D=0A
2. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg -5V)
3. Set Vd bias voltage to 0V *(pinch off test)* : I_D=0A
4. Apply Vd bias voltage (Typically: Vd = 20V)
5. Increase slowly Vg up to quiescent bias drain current Id=216mA
6. Put the RF input Power

“Power OFF” sequence

1. Remove RF input power
2. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -5V)
3. Decrease Vd bias voltage down to 0V
4. Turn Vg bias voltage to 0V

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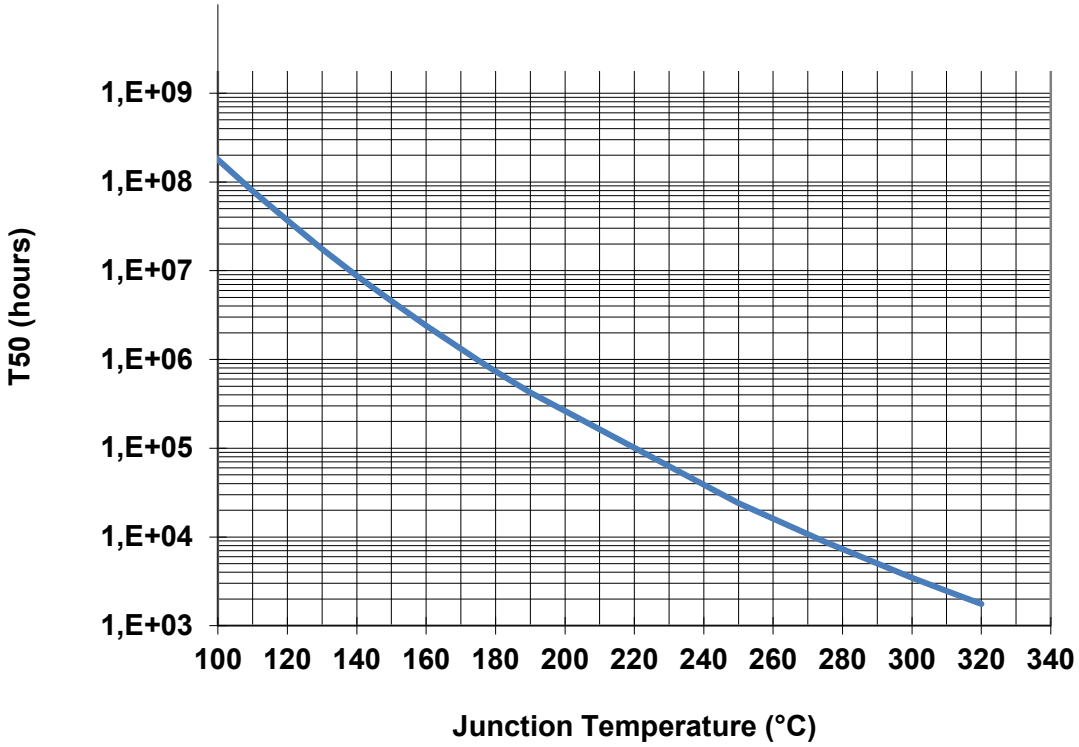
Device thermal performances

The device thermal performances below are based on UMS rules to evaluate the junction temperature.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA7062-QCB is manufactured.

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} [1] Thermal Resistance (Junction to Case)	Vd= 20V Id= 216mA Pout= 32dBm Pdiss= 8.66W CW	159	8.55	2.5E+6

[1] Assuming 85°C Tcase



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Typical Package Sij parameters

Tamb.= +25°C, Vd = +20V, Id = 216mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
1.0	-1.156	47.7	-80.264	-79.2	-56.906	58.4	-2.902	1.2
2.0	-1.605	-86.8	-73.044	-59.6	-34.942	-94.0	-3.885	135.0
3.0	-2.292	134.1	-68.668	119.8	-44.721	3.1	-2.237	-81.9
4.0	-5.229	-8.5	-69.527	-21.4	-48.589	-145.8	-1.867	106.6
5.0	-12.651	-123.9	-68.535	-135.8	-62.377	75.2	-1.772	-49.2
6.0	-10.246	157.3	-68.598	98.0	-53.071	53.2	-1.727	174.2
7.0	-7.789	41.9	-68.934	-38.1	-46.671	-82.8	-2.056	48.5
8.0	-7.313	-87.1	-70.253	-166.2	-43.740	134.2	-2.709	-91.7
9.0	-7.752	140.2	-73.237	78.6	-52.252	-3.5	-3.330	118.2
10.0	-7.564	-9.4	-67.549	12.3	-20.658	21.0	-9.93	44.7
11.0	-7.166	-144.6	-67.922	-110.4	-11.272	-112.2	-3.714	-124.1
12.0	-12.138	58.6	-62.745	114.8	10.409	8.5	-6.237	43.7
13.0	-25.317	-141.3	-66.392	-4.4	18.420	115.4	-11.222	167.6
14.0	-16.884	-0.7	-58.218	-123.6	19.028	-119.4	-10.453	-63.3
15.0	-22.232	160.0	-56.724	73.1	17.448	36.1	-8.262	170.2
16.0	-17.053	-10.3	-57.355	-82.2	16.922	-148.9	-10.203	49.0
17.0	-15.152	-154.2	-58.486	104.5	17.644	23.9	-12.881	-174.3
18.0	-22.373	49.9	-59.713	-76.5	18.712	-162.0	-7.482	45.1
19.0	-12.748	-150.5	-59.175	74.1	21.282	-0.2	-11.825	-110.0
20.0	-17.866	86.2	-57.653	-152.1	22.005	139.5	-8.498	13.0
21.0	-15.004	35.4	-56.914	-18.9	19.884	-82.0	-7.739	-97.2
22.0	-9.024	-96.7	-54.614	118.2	16.985	48.9	-9.650	-157.2
23.0	-7.285	103.7	-61.172	-105.5	8.145	152.1	-9.123	81.7
24.0	-4.942	-37.6	-75.387	166.9	-9.252	-57.4	-5.530	-118.4
25.0	-4.851	-155.7	-74.266	29.4	-24.372	146.5	-3.716	124.6
26.0	-5.790	78.8	-77.638	-64.0	-35.002	1.7	-4.219	14.5
27.0	-5.735	-63.7	-68.940	134.2	-44.474	-150.5	-6.297	-112.6
28.0	-5.014	176.9	-66.506	-37.2	-53.894	52.6	-6.708	77.4
29.0	-5.653	50.8	-67.021	174.4	-61.965	-108.1	-3.558	-40.3
30.0	-4.787	-67.2	-63.903	84.9	-63.500	99.8	-3.652	-126.5

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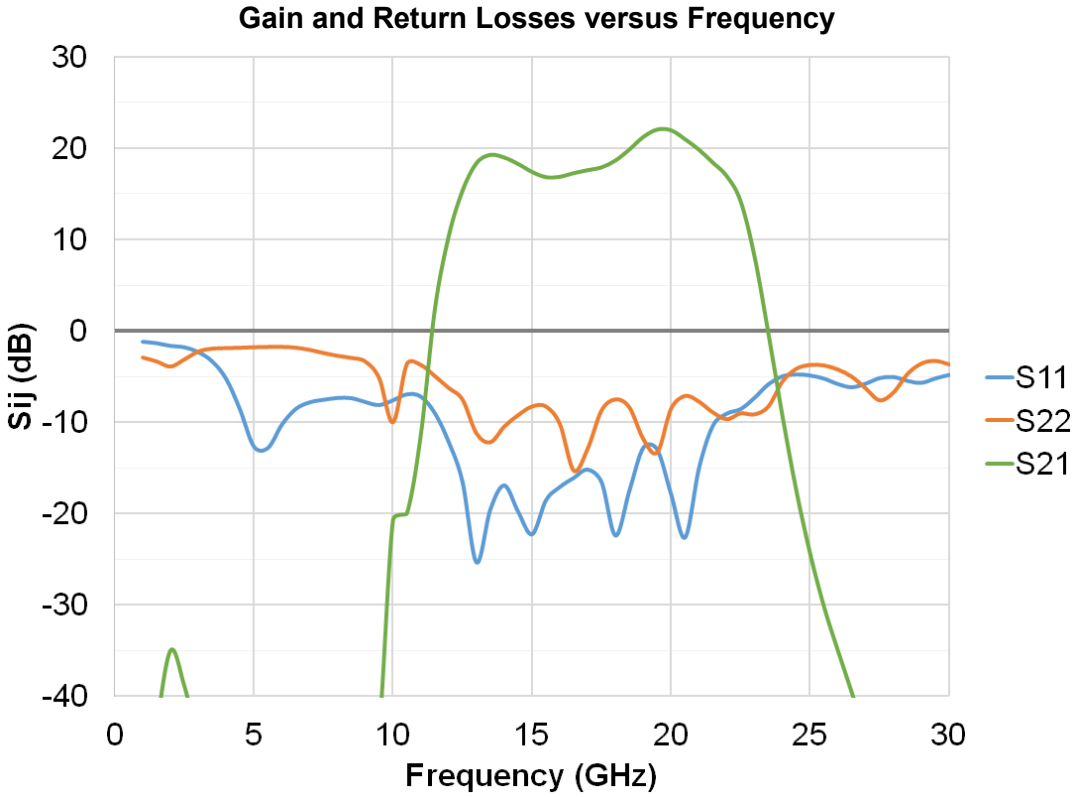
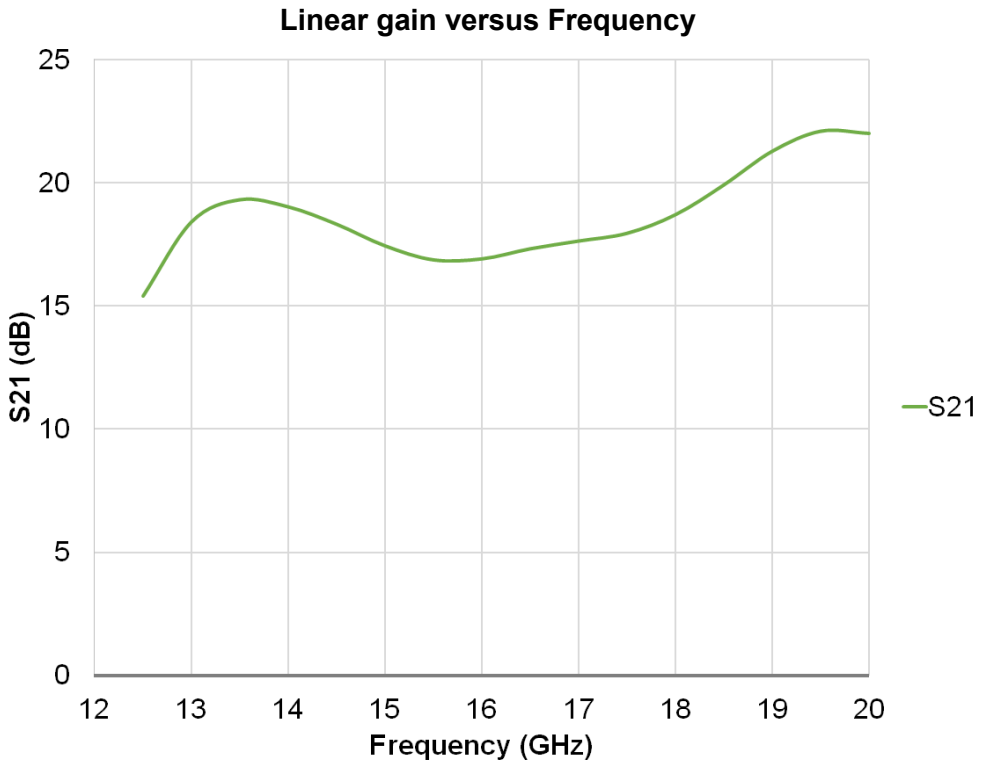
Typical Board Measurements

Tamb.= +25°C, Vd = +20V, Id = 216mA





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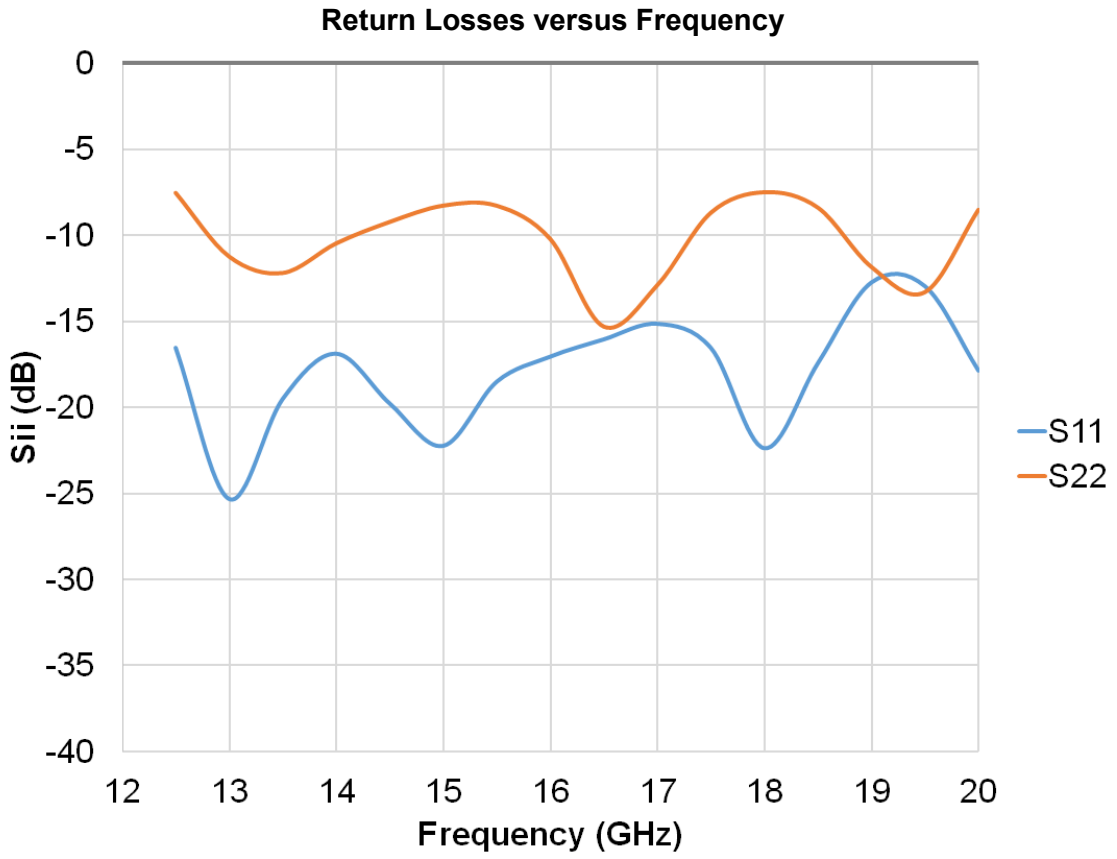
Typical on Board Measurements

Tamb.= +25°C, Vd = +20V, Id = 216mA



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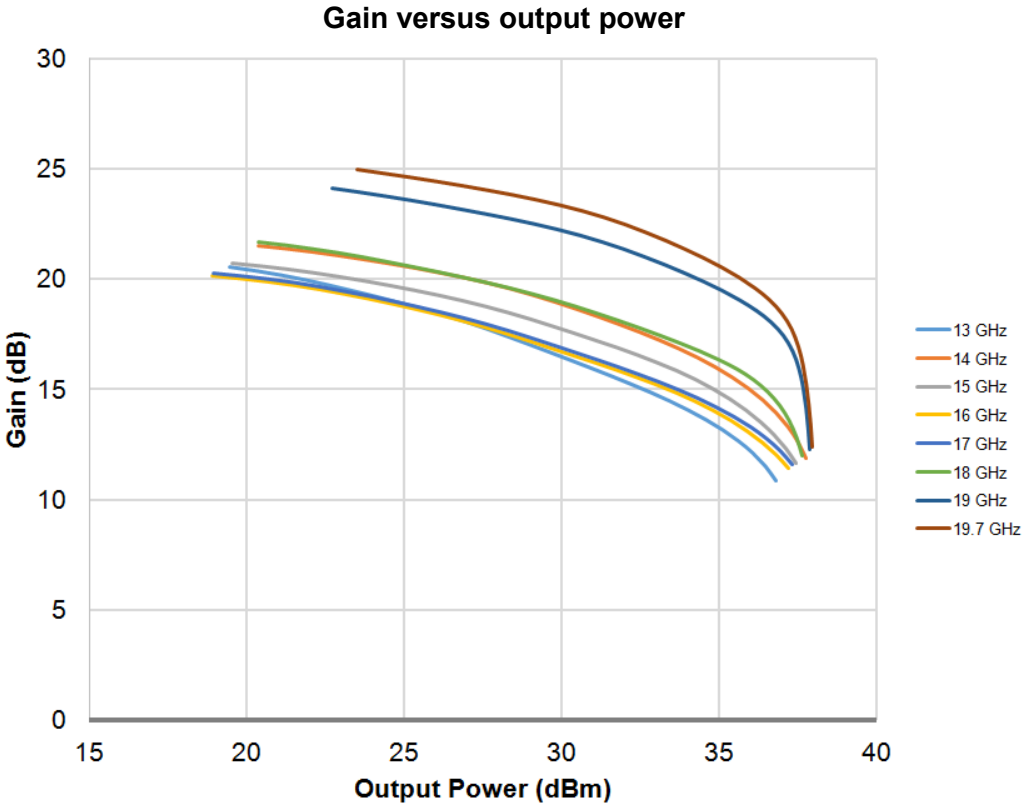
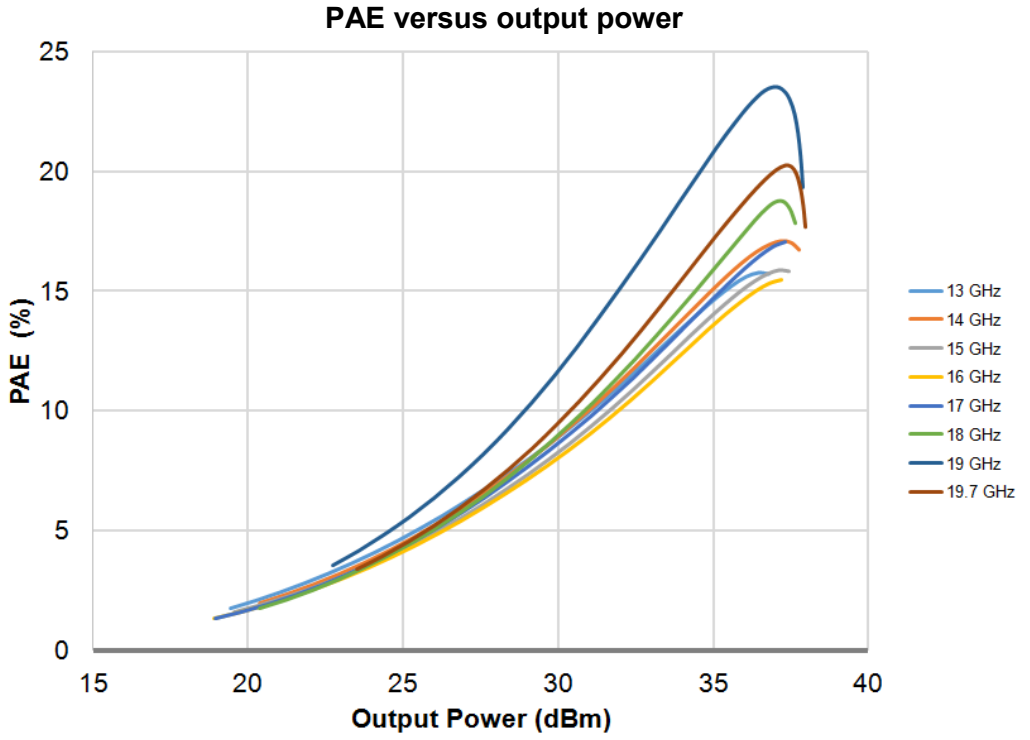
Typical Board Measurements

Tamb.= +25°C, Vd = +20V, Id = 216mA





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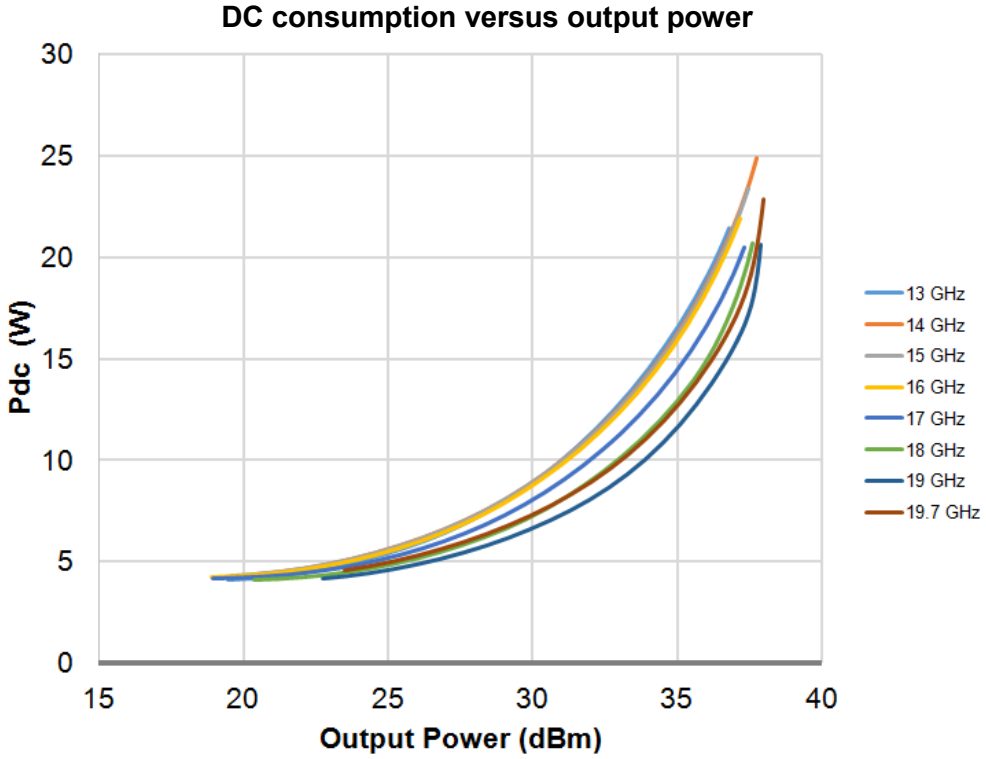
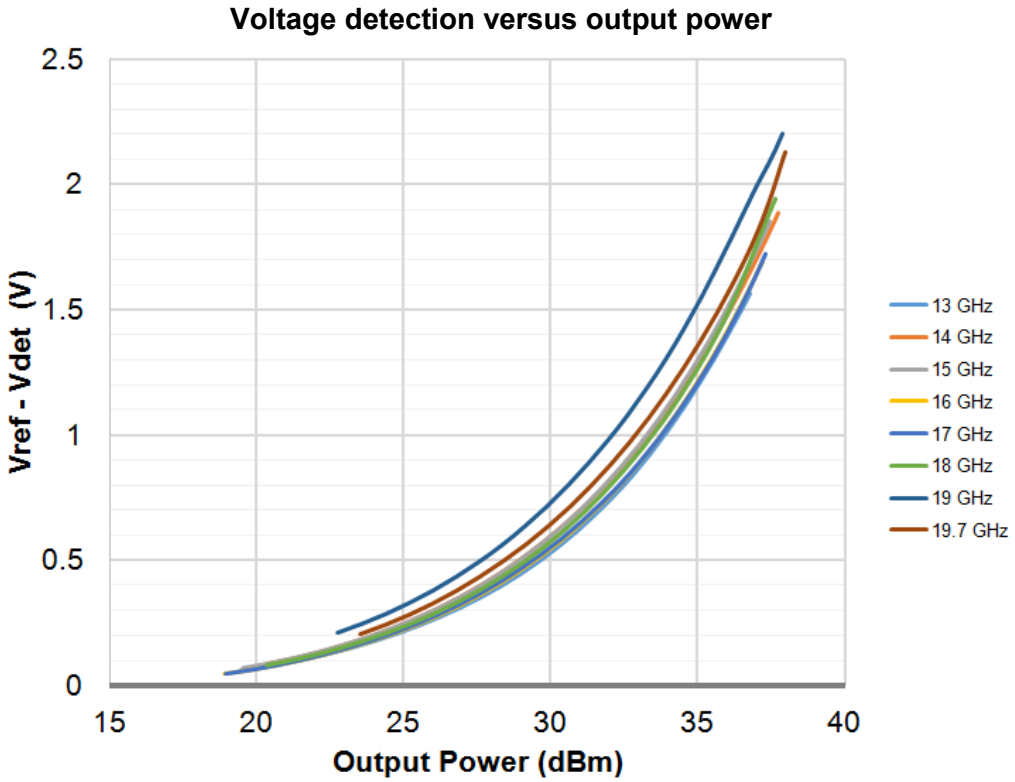
Tamb.= +25°C, Vd = +20V, Id = 216mA





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Typical Board Measurements

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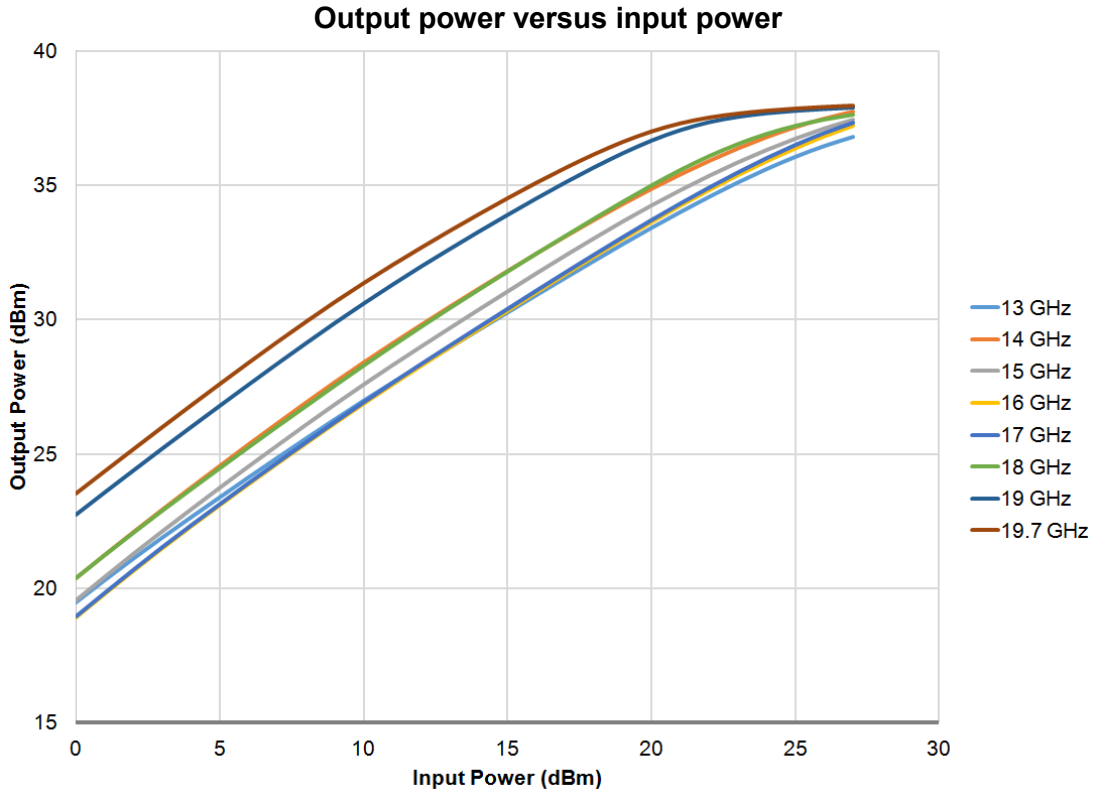

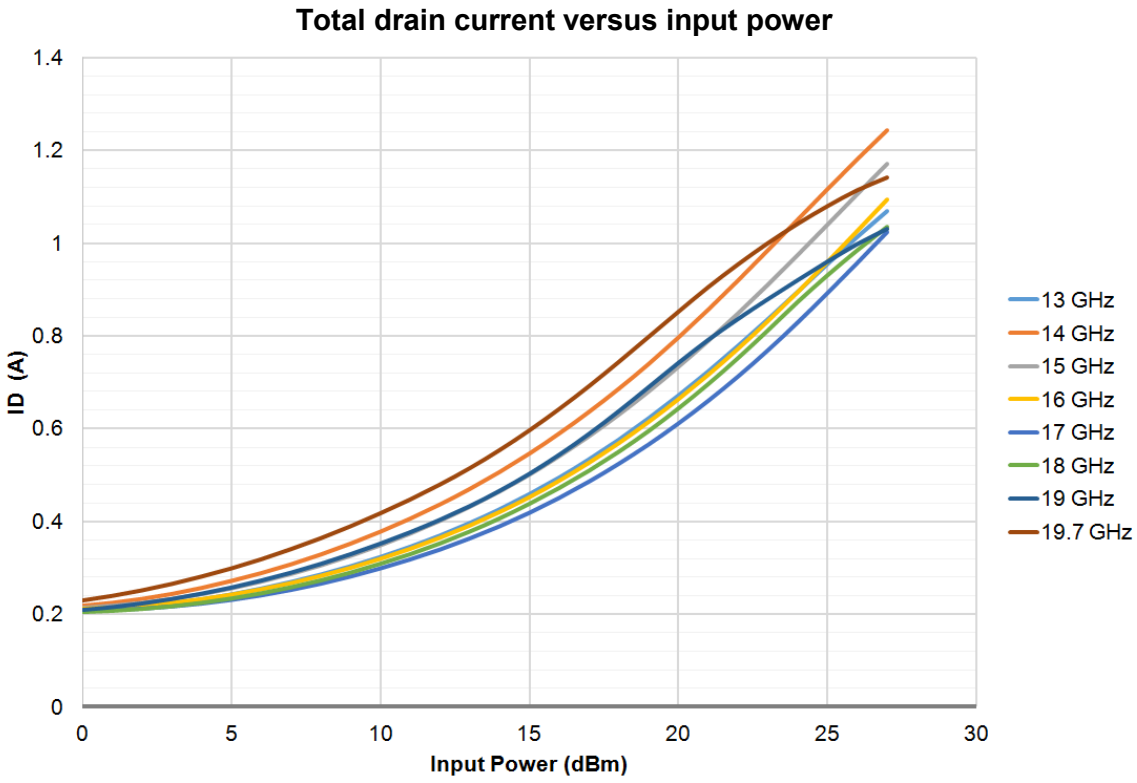

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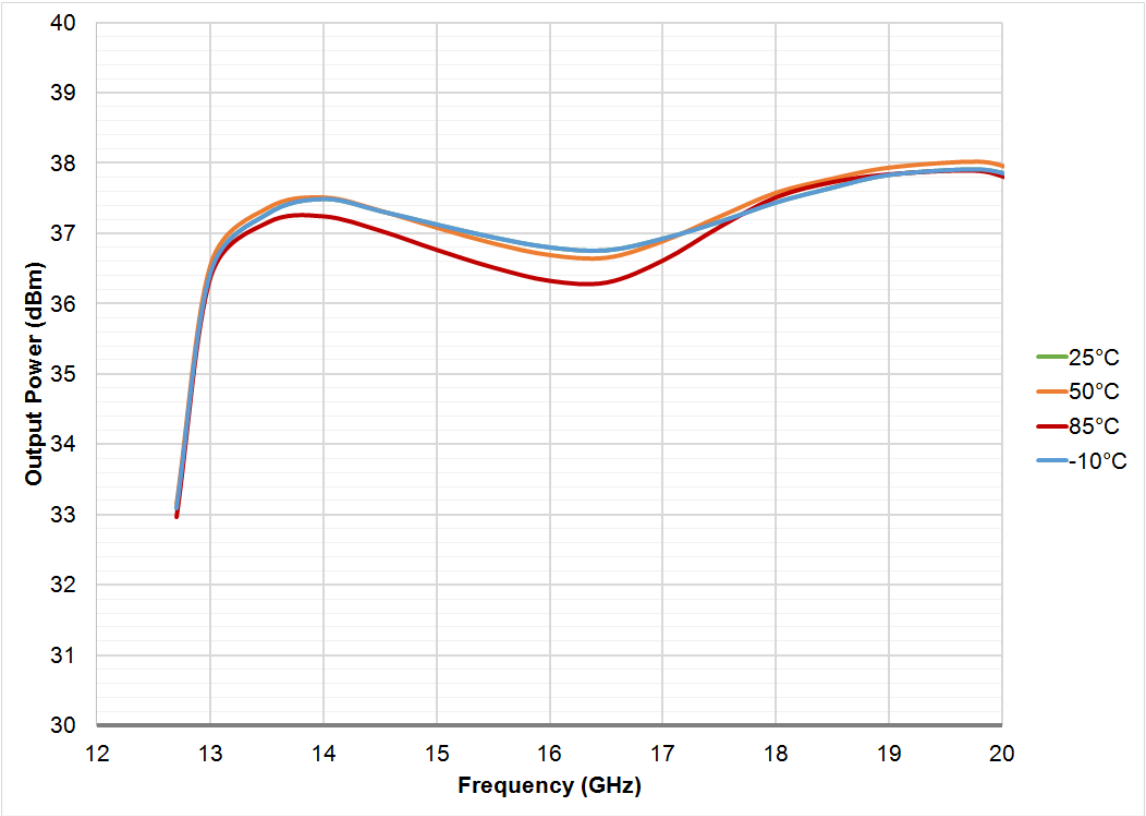
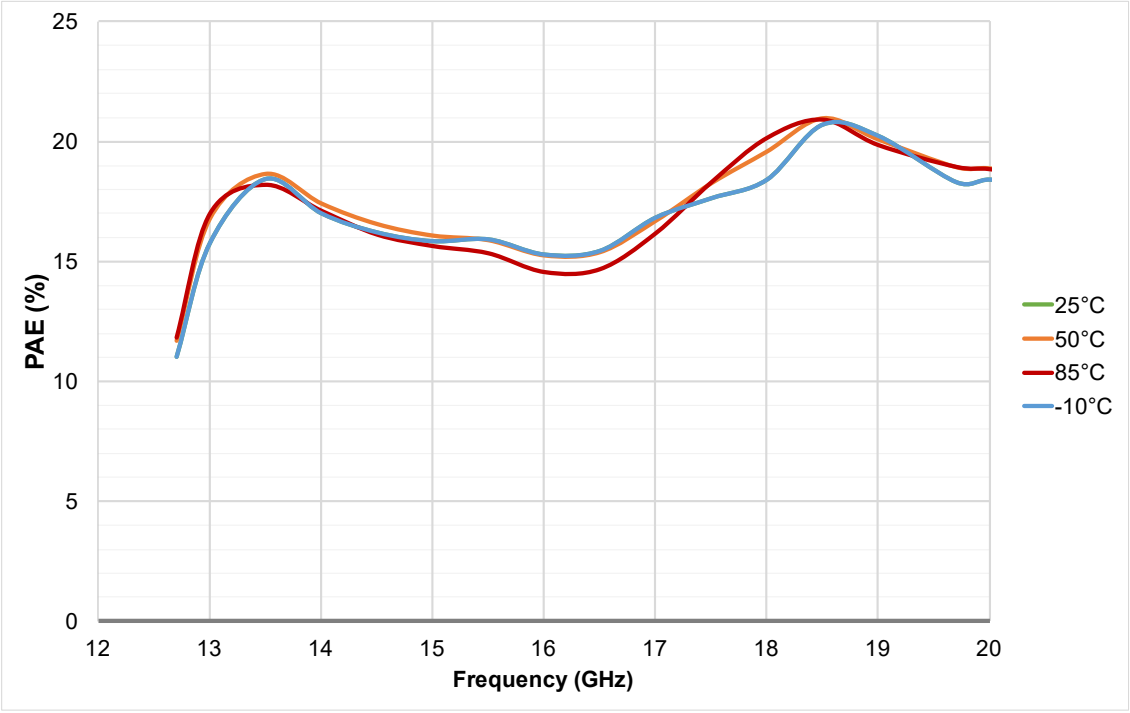
Typical Board Measurements

Tamb.= +25°C, Vd = +20V, Id = 216mA

Saturated output power versus frequency & temperature



PAE at saturation level versus frequency & temperature



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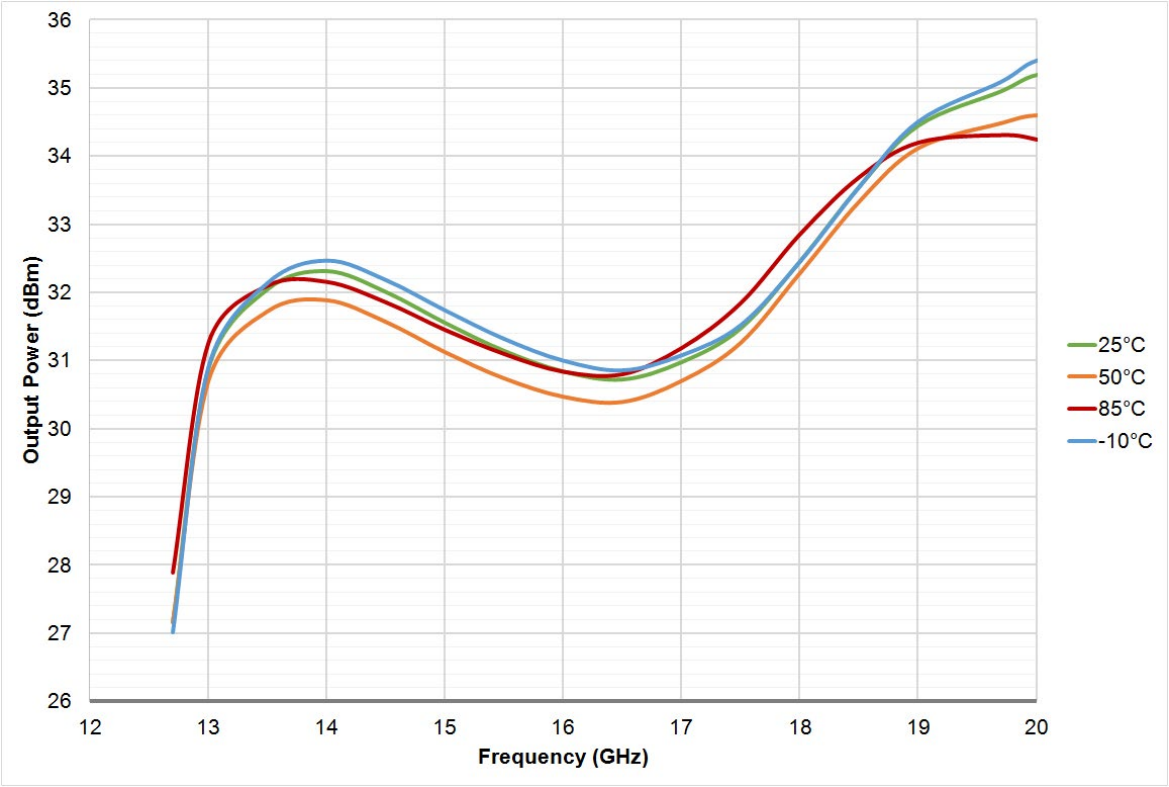
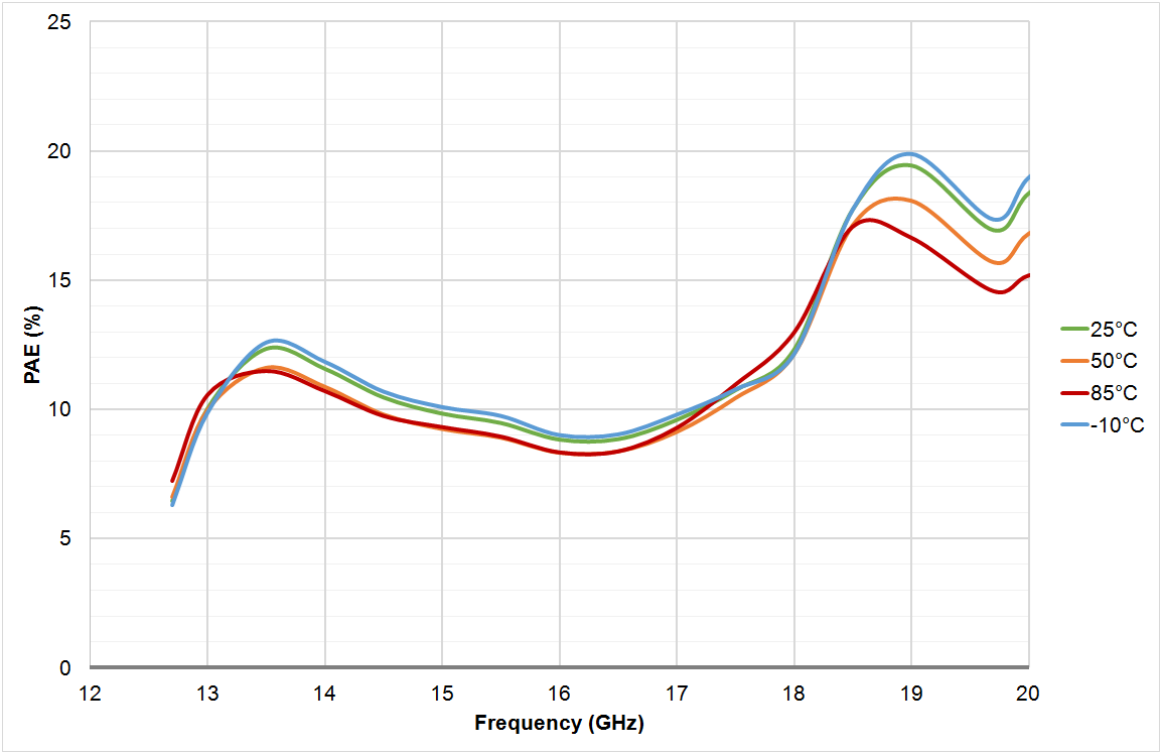
Typical Board Measurements

Tamb.= +25°C, Vd = +20V, Id = 216mA

Output power at 6dB output back-off versus frequency & temperature



PAE at 6dB output back-off versus frequency & temperature



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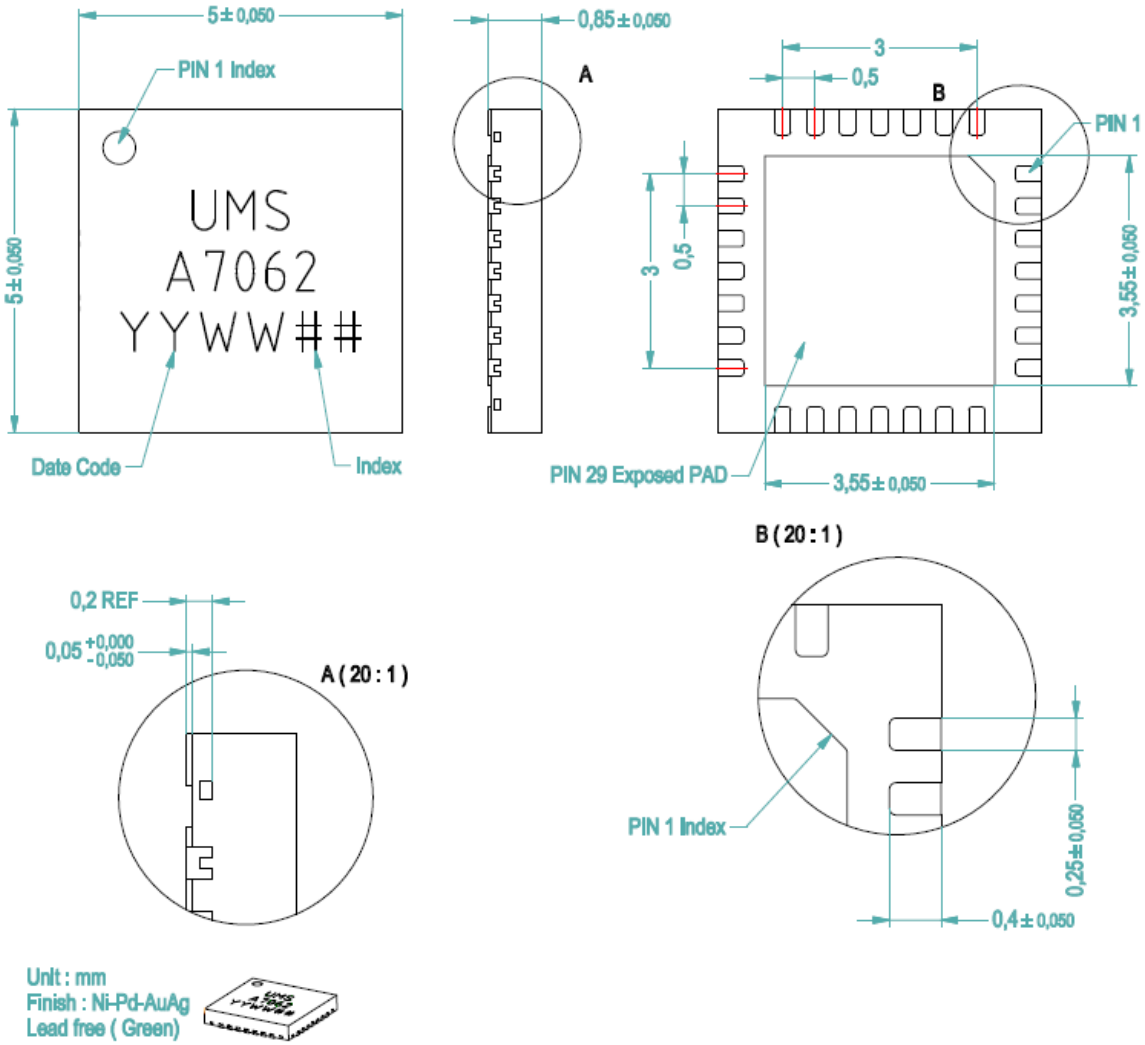
Package outline (1)



Ni-Pd-Au-Ag Lead free	(Green)	1- Nc	11- Vg2	21- Vc
Units :	mm	2- Nc	12- Gnd(2)	22- Det
From the standard :	JEDEC MO-220	3- Nc	13- Vd2	23- Vd2
	(VGGD)	4- RF in	14- SH	24- G_ref
		5- Nc	15- Nc	25- Vg2
		6- Nc	16- Nc	26- Gnd(2)
		7- Nc	17- Nc	27- Vd1
		8- Vg1	18- RF out	28- Vg1
		9- Vd1	19- Nc	29- Gnd
		10- Gnd(2)	20- Ref	

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (https://www.ums-rf.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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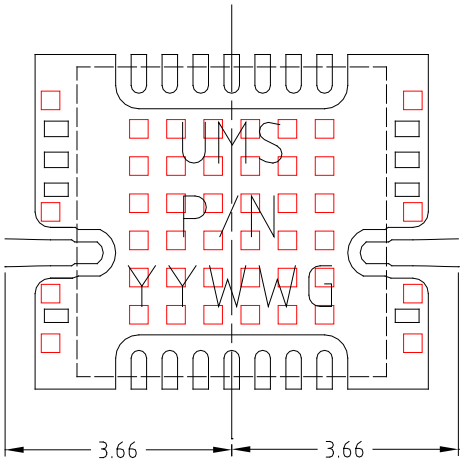
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.66mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation board recommended in paragraph "Evaluation board".



Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% Ni-Pd-Au-Ag
MSL Rating	MSL3

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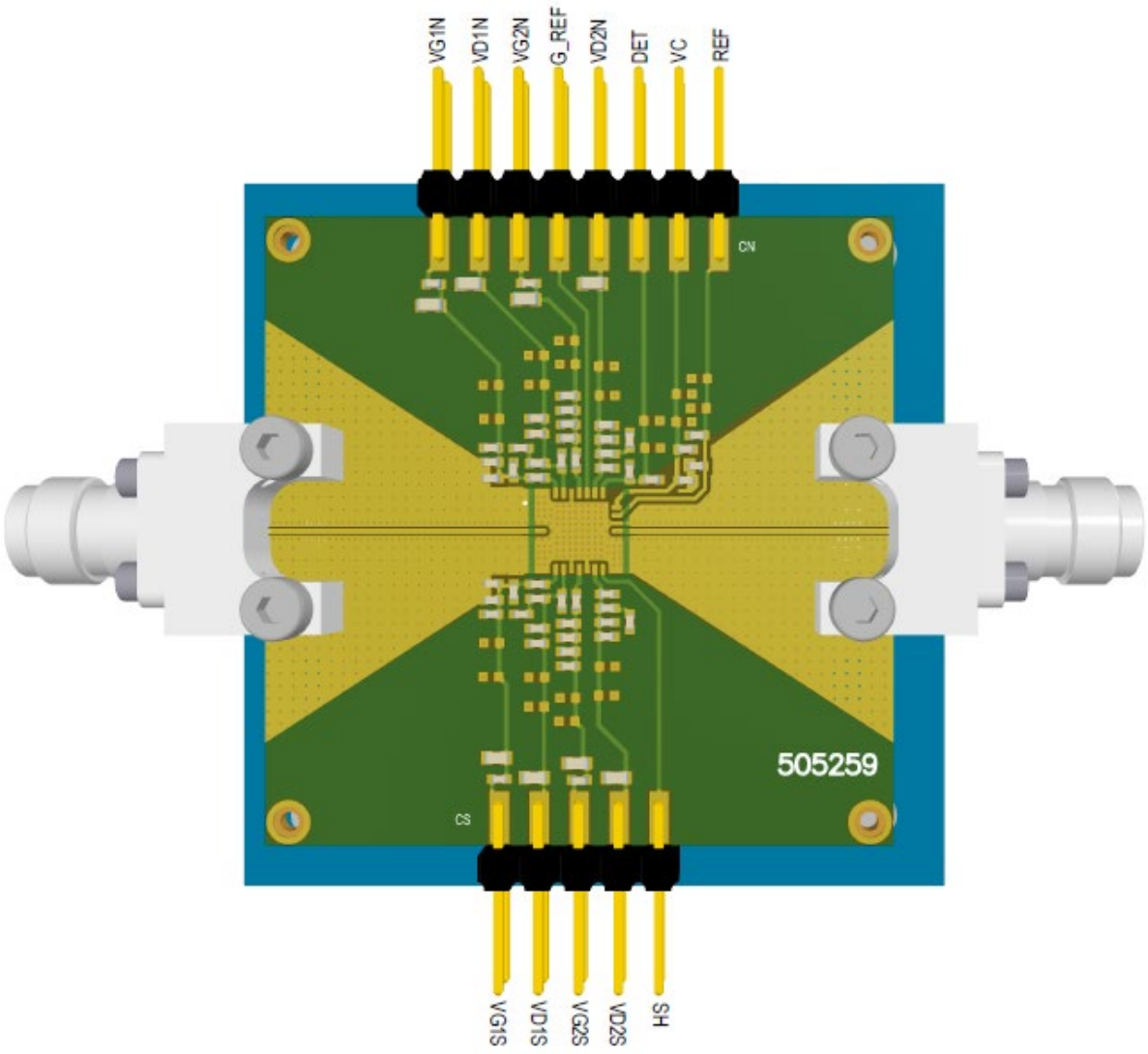
Evaluation board

- Compatible with the proposed footprint.
- Based on typically Ro4350 / 10mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF ±5%, 10nF ±10% and 1µF ±10% are recommended for all HPA DC accesses.
- 10kΩ resistor in parallel with 100pF ±5% capacitors is recommended for REF and DET accesses.
- See application note AN0017 for details.



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

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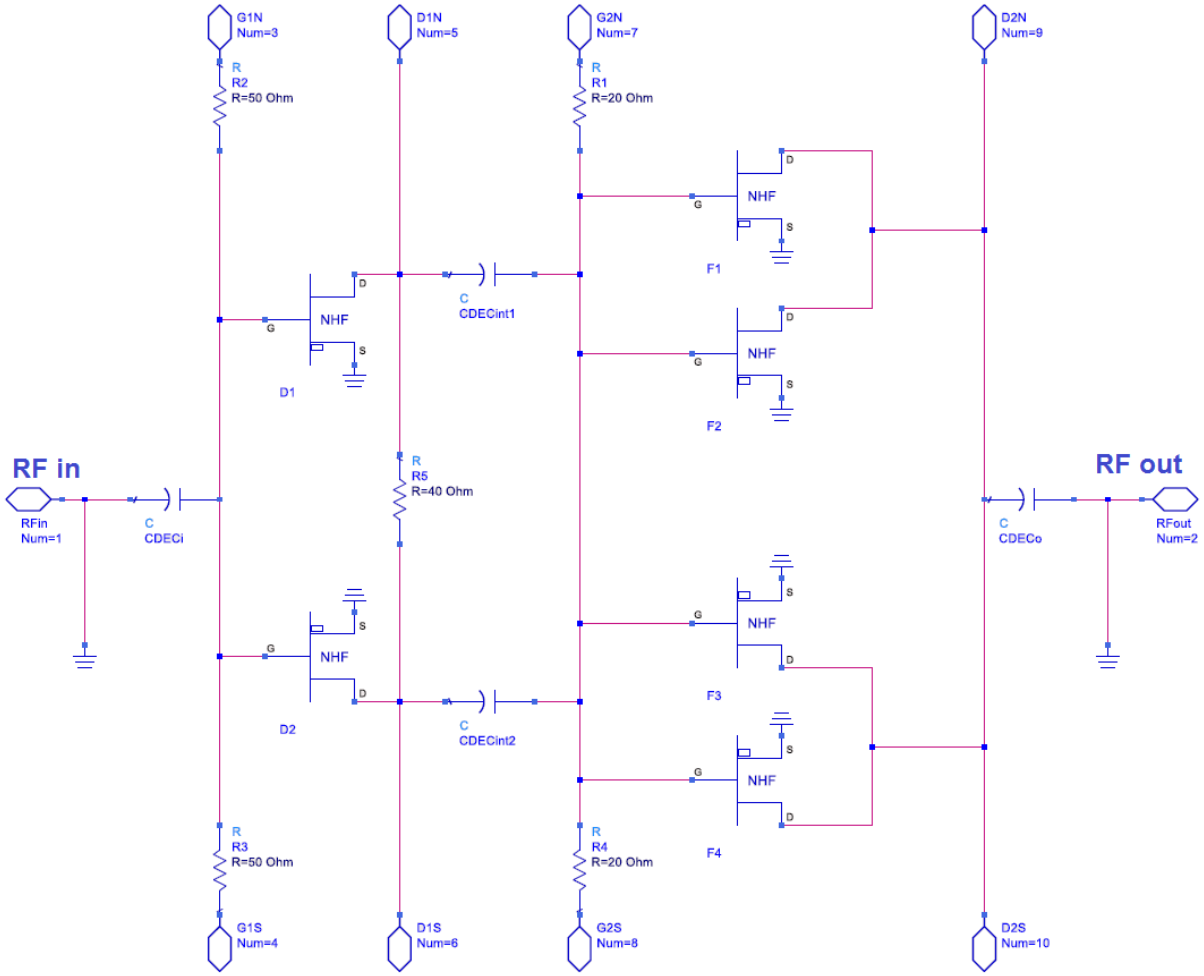
DC Schematic



Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

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Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 at https://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 5x5 package:	CHA7062-QCB/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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